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METHOD FOR FABRICATING SEMICONDUCTOR DEVICE HAVING GROUP III NITRIDE

BACKGROUND OF THE INVENTION

The present invention relates to a method for fabricating a semiconductor device of Group III nitride semiconductors.

A Group III nitride semiconductor, which is expressed by the general formula of $Al_xGa_{1-x-y}In_yN$ (where $0 \leqq x \leqq 1$, $0 \leqq y \leqq 1$ and $x+y \leqq 1$) has a direct-transition-type band structure with a band gap energy ranging from about 1.9 eV to about 6.2 eV and excels in thermal resistance. Therefore, semiconductor devices made of these Group III nitride semiconductors are currently under vigorous research and development. A semiconductor light-emitting device made of compound semiconductors mainly containing gallium nitride, for example, attracts increasing attention as a strong candidate for a light source of a next-generation high-density optical disk or a full-color LED display.

To improve the operating performance of such a light-emitting device made of Group III nitride semiconductors, it is extremely important how to form a p-type semiconductor layer with a low resistance.

Hereinafter, a conventional method for forming a p-type semiconductor layer and a semiconductor device using such a layer will be exemplified with reference to FIG. **10**.

FIG. **10** illustrates a partial cross section of a conventional semiconductor device. As shown in FIG. **10**, a buffer layer **102** of aluminum nitride (AlN) or gallium nitride (GaN) is formed on a sapphire substrate **101**. A first semiconductor layer **103** of undoped GaN is formed on the buffer layer **102**. A second semiconductor layer **104** of p-type GaN doped with magnesium (Mg) as an acceptor is formed on the first semiconductor layer **103**. A p-side electrode **105** is formed on the second semiconductor layer **104** by alternately stacking nickel (Ni) and gold (Au) layers **105***a* and **105***b* one upon the other. In this example, only the method for forming the second semiconductor layer **104** will be specifically described and the illustration of an n-side electrode is omitted in FIG. **10**.

Examples of the p-type dopant include magnesium (Mg), zinc (Zn), calcium (Ca), strontium (Sr) and beryllium (Be). Among these elements, Mg and Zn are used particularly often.

Generally speaking, even if the second semiconductor layer **104** is doped with a p-type dopant, the p-type dopant can hardly act as an acceptor as it is (i.e., without any special treatment). Thus, the second semiconductor layer **104** is composed of intrinsic (i-type) crystals with a resistivity as high as 1×10^8 Ωcm or more. It is believed that this is because hydrogen, which is released due to the decomposition of ammonium (NH_3) gas used as a nitride source in growing the second semiconductor layer **104**, is bonded to a p-type dopant such as Mg or Zn to inhibit the acceptor action of the dopant.

Thus, various methods for forming a p-type semiconductor layer by making the p-type dopant introduced act as an acceptor, i.e., by activating the dopant, have already been proposed.

According to a first exemplary method, the second semiconductor layer **104** doped with a p-type dopant is exposed to an electron beam as disclosed in Japanese Patent Publication for Opposition No. 6-9258.

A second exemplary method is disclosed in Japanese Laid-Open Publication No. 8-213656, for example. According to the second method, the second semiconductor layer **104** is heated up to about 800° C. within an inert gas ambient.

The electrical energy of the electrons in the electron beam irradiated according to the first method or the thermal energy created according to the second method might dissociate hydrogen, which has been bonded to the p-type dopant such as Mg or Zn, from the dopant. Then, that dissociated hydrogen might detach itself from the second semiconductor layer **104**, thereby possibly activating the p-type dopant as an acceptor.

According to a third exemplary method as disclosed in Japanese Laid-Open Publications Nos. 6-275868 and 10-163529, the second semiconductor layer **104** is annealed within nitrogen ambient and oxygen ambient, respectively, to activate Mg in the second semiconductor layer **104**.

A fourth exemplary method is disclosed in Japanese Laid-Open Publication No. 10-144960, for example, in which the second semiconductor layer **104** is plasma annealed.

According to any of these proposed methods for forming a p-type semiconductor layer, the second semiconductor layer **104** shows a resistivity of about 1 Ωcm and a p-side electrode **105** can be in ohmic contact with the second semiconductor layer **104** at a contact resistivity of about 1×10^{-3} Ωcm^2.

These conventional methods for forming a p-type semiconductor layer among Group III nitride semiconductor layers, however, have the following drawbacks.

According to the first method, the electron beam irradiated has a spot diameter of at most 50 to 60 μm. Thus, when the substrate **101** has a size of approximately 2 centimeters square, it takes more than 10 hours to expose the entire upper surface of the second semiconductor layer **104** to the electron beam, or to finish processing a single substrate **101**. Therefore, it is difficult to apply such a method to mass production, and it is impossible to process a plurality of substrates **101** in parallel.

Under the second and third methods, the second semiconductor layer **104** does not show p-type conductivity unless the temperature of the substrate is raised to as high as 600° C. or higher. In annealing the substrate to raise its temperature to 600° C. or higher, however, defects or cracking might be caused in the first or second semiconductor layer **103** or **104** depending on the thermal hysteresis before and after the annealing process. This is because the thermal expansion coefficient of the sapphire substrate **101** is much different from that of the first and second semiconductor layers **103** and **104** of GaN. In addition, if the temperature of the substrate **101** reaches 600° C. or higher, nitrogen might detach itself from the first and second semiconductor layers **103** and **104** or Mg might thermally diffuse from the second semiconductor layer **104** into the first semiconductor layer **103**, thus deteriorating the crystallinity of these semiconductor layers. As a result, the performance of the semiconductor device with such layers also deteriorates.

As for the fourth method, no specific details about plasma annealing are available from the disclosure of the above-cited reference.

SUMMARY OF THE INVENTION

An object of the present invention is forming a p-type layer with a low resistance out of a Group III nitride semiconductor layer in a short time with substantially no defects caused in the semiconductor layer.

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A first exemplary method for fabricating a semiconductor device according to the present invention includes the steps of: a) forming a semiconductor layer of a Group III nitride containing a dopant over a substrate; and b) exposing the semiconductor layer to a plasma with the temperature of the substrate kept at about 600° C. or lower, thereby making the conductivity type of the semiconductor layer p-type.

According to the first method, the plasma is highly reactive even at a relatively low temperature and can effectively dissociate the bond of a dopant atom to a hydrogen atom, which usually prevents the dopant from being activated as an acceptor. Thus, no defects or cracking is caused in the semiconductor layer due to the thermal hysteresis, and no dopants diffuse from the resultant p-type semiconductor layer into other adjacent semiconductor layers, either. In addition, the processing time per substrate can be shortened and a plurality of substrates can be processed in parallel by using the plasma, thus further increasing the processing efficiency.

In one embodiment of the present invention, the first method preferably further includes the step of c) forming a p-side electrode out of a metal on the semiconductor layer after the step b) has been performed.

In such an embodiment, the resulting p-side electrode can be in ohmic contact with the p-type semiconductor layer with much more certainty, because the electrode is formed on the high-quality semiconductor layer that has been turned into p-type efficiently. As a result, a semiconductor device of quality can be fabricated efficiently.

In this particular embodiment, the step c) may include annealing the p-side electrode at about 400° C. or lower after the p-side electrode has been formed.

In such an embodiment, the p-side electrode can be alloyed with the semiconductor layer without damaging the crystallinity of the semiconductor layer.

In an alternate embodiment, the step c) may include exposing the semiconductor layer to a plasma after the p-side electrode has been formed.

In such an embodiment, the dopant remaining in the semiconductor layer can be further activated after the p-side electrode has been formed thereon.

In another embodiment of the present invention, the plasma is preferably generated by an RF, ECR or hot-wall process.

In such an embodiment, the plasma can be generated just as intended.

In still another embodiment, the plasma preferably comprises nitrogen plasma.

In such an embodiment, it is possible to prevent nitrogen from detaching itself from the semiconductor layer during the exposure of the nitrogen-containing semiconductor layer to the plasma. Thus, the crystallinity of the semiconductor layer can be kept excellent.

In still another embodiment, the dopant is preferably selected from the group consisting of magnesium (Mg), zinc (Zn), calcium (Ca), strontium (Sr), beryllium (Be), cadmium (Cd), mercury (Hg) and lithium (Li).

In such an embodiment, the semiconductor layer can be turned into p-type with more certainty.

A second exemplary method for fabricating a semiconductor device according to the present invention includes the steps of: a) forming a semiconductor layer of a Group III nitride containing a dopant over a substrate; b) forming a p-side electrode out of a metal on the semiconductor layer; and c) exposing the semiconductor layer to a plasma with the temperature of the substrate kept at about 600° C. or lower after the step b) has been performed, thereby making the conductivity type of the semiconductor layer p-type.

According to the second method, it is possible to effectively dissociate the bond of a dopant atom to a hydrogen atom, for example. Thus, no defects or cracking is caused in the semiconductor layer due to the thermal hysteresis, and no dopants diffuse from the resultant p-type semiconductor layer into other adjacent semiconductor layers, either. In addition, the resulting p-type semiconductor layer can be alloyed with the p-side electrode at the same time.

In one embodiment of the present invention, the metal is preferably selected from the group consisting of nickel (Ni), iron (Fe), copper (Cu), chromium (Cr), tantalum (Ta), vanadium (V), manganese (Mn), aluminum (Al), silver (Ag), palladium (Pd), iridium (Ir), gold (Au) and platinum (Pt).

In such an embodiment, the p-side electrode can be formed on the p-type semiconductor layer of a Group III nitride just as intended.

In another embodiment, the metal is preferably a hydrogen-storing metal selected from the group consisting of titanium (Ti), magnesium (Mg), calcium (Ca), zirconium (Zr), lanthanum (La), niobium (Nb), vanadium (V), nickel (Ni), iron (Fe), manganese (Mn), cobalt (Co), chromium (Cr) and aluminum (Al).

In such an embodiment, since the p-side electrode is made of a hydrogen-storing metal, hydrogen atoms, which have detached themselves from the semiconductor layer, are stored in the hydrogen-storing metal. Accordingly, it is possible to prevent the hydrogen atoms detached from being recombined with the p-type dopant in the semiconductor layer. As a result, the acceptor in the resulting p-type semiconductor layer can be activated at a sufficiently high rate.

In still another embodiment, the step b) preferably includes forming a hydrogen-adsorbing layer out of a hydrogen-storing metal on the semiconductor layer before the p-side electrode is formed.

In such an embodiment, since the hydrogen-adsorbing layer is formed between the p-side electrode and the semiconductor layer, hydrogen atoms, which have detached themselves from the semiconductor layer, are stored in the hydrogen-adsorbing layer. Accordingly, it is possible to prevent the hydrogen atoms detached from being recombined with the p-type dopant in the semiconductor layer. As a result, the acceptor in the resulting p-type semiconductor layer can be activated at a sufficiently high rate.

In this particular embodiment, the hydrogen-storing metal is preferably selected from the group consisting of titanium (Ti), magnesium (Mg), calcium (Ca), zirconium (Zr), lanthanum (La), niobium (Nb), vanadium (V), nickel (Ni), iron (Fe), manganese (Mn), cobalt (Co), chromium (Cr) and aluminum (Al).

In still another embodiment, the plasma preferably comprises nitrogen plasma.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1(*a*) and 1(*b*) are cross-sectional views illustrating respective process steps for fabricating a semiconductor device according to a first embodiment of the present invention.

FIG. 2 is a cross-sectional view illustrating another process step for fabricating a semiconductor device according to the first embodiment.

FIG. 3 is a schematic cross-sectional view illustrating a plasma processor for use in the method for fabricating a semiconductor device according to the first embodiment.

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FIG. **4** is a graph illustrating the dependence of a contact resistivity between a p-side electrode and a p-type semiconductor layer on the plasma processing time in the method according to the first embodiment.

FIG. **5** is a graph illustrating the dependence of the resistivity of a semiconductor device fabricated by the method according to the first embodiment on the plasma processing time.

FIG. **6** is a graph illustrating respective photoluminescence intensities of a semiconductor layer that has not been processed with plasma yet and a plasma-processed semiconductor layer in the method according to the first embodiment.

FIG. **7** is a graph illustrating respective dependence of a carrier density on an annealing temperature for the semiconductor layer processed with plasma by the method according to the first embodiment and a semiconductor layer annealed by a conventional method.

FIGS. **8**(*a*) and **8**(*b*) are cross-sectional views illustrating respective process steps for fabricating a semiconductor device according to a second embodiment of the present invention.

FIG. **9** is a cross-sectional view illustrating another process step for fabricating a semiconductor device according to the second embodiment.

FIG. **10** is a cross-sectional view illustrating part of a conventional semiconductor device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment 1

Hereinafter, a first exemplary embodiment of the present invention will be described with reference to the accompanying drawings.

FIGS. **1**(*a*), **1**(*b*) and **2** illustrate cross-sectional structures illustrating respective process steps for fabricating a double-heterojunction nitride semiconductor laser device according to the first embodiment.

As shown in FIG. **1**(*a*), respective epitaxial layers are sequentially grown by metalorganic vapor phase epitaxy (MOVPE), for example, on a principal surface of a sapphire substrate **11**, which is a (0001) crystallographic plane. The MOVPE process may be performed under the conditions that trimethylaluminum (TMA), trimethylgallium (TMG) or trimethylindium (TMI) is used as a Group III element source, ammonium (NH_3) is used as a nitrogen source, hydrogen is supplied as a carrier gas and the pressure is kept at about 50 Torr (where 1 Torr is approximately equal to 133.3 Pa).

Specifically, first, an AlN buffer layer **12** is grown on the substrate **11** to a thickness of about 40 nm using TMA and NH_3 as source materials and keeping a crystal growth temperature at about 500° C. Next, an n-type GaN contact layer **13** is grown to a thickness of about 1.0 μm while raising the growth temperature up to 1000° C., changing the Group III element source from TMA into TMG, and adding silicon (Si) as an n-type dopant. Thereafter, an n-type AlGaN cladding layer **14** is grown to be about 0.7 μm thick while adding an appropriate amount of TMA to TMG. Then, an InGaN multiple quantum well active layer **15** is grown to be about 50 nm thick in total with the growth temperature lowered to about 800° C. and an appropriate amount of TMI added instead of TMA. Next, a first Mg-doped layer **16**A of AlGaN is grown to be about 0.7 μm thick while raising the growth temperature to about 1000° C., stopping the supply of the n-type dopant, adding cyclopentadienylmagnesium (Cp_2Mg), containing Mg as a p-type dopant, and supplying an appropriate amount of TMA instead of TMI. Then, a second Mg-doped layer **17**A of GaN is grown to a thickness of about 1.0 μm using only TMG as the Group III element source. An epitaxial substrate **20** is obtained in this manner. The concentration of Mg in the second Mg-doped layer **17**A is set at about 2×10^{19} cm^{-3}. In this case, hydrogen, which has been released by the decomposition of NH_3, as the nitrogen source, is bonded to Mg contained in the first and second Mg-doped layers **16**A and **17**A.

Then, the epitaxial substrate **20**, on which the respective layers **12**, **13**, **14**, **15**, **16**A and **17**A have been stacked, is introduced into a plasma processor.

Next, a plasma processor according to the first embodiment will be described with reference to FIG. **3**. FIG. **3** schematically illustrates a cross section of a plasma processor **50** according to the first embodiment. As shown in FIG. **3**, the plasma processor **50** includes: a vacuum chamber (i.e., a reaction chamber) **51** with gas inlet and outlet ports **52**A and **52**B in a pair of opposite walls; and upper and lower electrodes **53**A and **53**B, which are provided on the upper and lower bottoms of the chamber **51** to face each other and can be heated. The upper electrode **53**A is grounded, while the lower electrode **53**B is connected to an RF power supply **55** via a matcher **54**. The matcher **54** and the RF power supply **55** are both provided outside of the vacuum chamber **51**. As can be seen, the plasma processor **50** is a so-called "parallel-plate plasma generator".

One or two epitaxial substrates **20** shown in FIG. **1**(*a*) are placed on the lower electrode **53**B of the plasma processor **50** such that the respective upper surfaces of the substrates **20** are uniformly exposed to plasma. Thereafter, the vacuum chamber **51** is evacuated with the temperature of the substrates kept at room temperature. Subsequently, the pressure inside the chamber **51** is adjusted at about 2×10^{-2} Torr with the flow rate of nitrogen gas set at about 5 sccm.

Next, plasma discharge is caused inside the vacuum chamber **51** with an RF power of 150 W or less supplied at 13.56 MHz, thereby filling the vacuum chamber **51** with nitrogen plasma. The epitaxial substrates **20** are exposed to this nitrogen plasma for about 40 minutes.

As a result, Mg, which has been introduced as an acceptor into the first and second Mg-doped layers **16**A and **17**A, is sufficiently activated even around room temperature. Accordingly, p-type cladding layer **16**B and p-type contact layer **17**B, which both have a low resistance and excellent crystallinity, are formed out of the first and second Mg-doped layers **16**A and **17**A, respectively, as shown in FIG. **1**(*b*).

Next, the epitaxial substrate **20**, including the p-type layers with a reduced resistance, is introduced into an evaporation system (not shown). First and second metal films **18***a* and **18***b* of Ni and Au are deposited on the p-type contact layer **17**B in this order to be about 100 nm thick in total, thereby forming a p-side electrode **18** as shown in FIG. **2**.

Then, the respective epitaxial layers **13**, **14**, **15**, **16**B and **17**B on the epitaxial substrate **20** are dry-etched anisotropically, thereby partially exposing the n-type contact layer **13**. And first and second metal films **19***a* and **19***b* of Ti and Au are deposited on the exposed surface of the n-type contact layer **13** in this order to be about 100 nm thick in total, thereby forming an n-side electrode **19**.

Thereafter, the epitaxial substrate **20**, on which these electrode prototype films have been deposited, is annealed at about 400° C. within a nitrogen ambient, thereby alloying the electrode prototype films with the respective semiconductor layers adjacent to these films.

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It should be noted that the p-side electrode **18** may be alloyed with the contact layer **17B** before the n-side electrode **19** is formed.

As described above, the acceptor Mg is activated according to this embodiment by exposing the first and second Mg-doped layers **16A** and **17A** to the nitrogen plasma. Thus, the number of defects or cracks, which are usually caused in the epitaxial layers due to the thermal hysteresis, can be drastically reduced. Also, the acceptor Mg is much less likely to thermally diffuse from the first Mg-doped layer **16A** into the active layer **15**. As a result, the operating performance of the semiconductor laser device can be enhanced. In addition, a plurality of substrates can be processed at the same time to activate the acceptor, thus increasing the throughput.

The plasma source does not have to be nitrogen gas. However, since it is possible to prevent nitrogen from detaching itself from the first and second Mg-doped layers **16A** and **17A** when the nitrogen plasma is used, the performance of the semiconductor laser device can be further improved.

FIG. **4** illustrates the dependence of a contact resistivity between the p-side electrode **18** and the p-type contact layer **17B** on the plasma processing time. FIG. **5** illustrates the dependence of the resistivity of the semiconductor laser device on the plasma processing time. In the illustrated example, the contact resistivity and the resistivity are measured by a transmission line model (TLM) method.

As shown in FIG. **4**, the contact resistivity is always lower than 1×10^{-3} Ωcm^2, and it can be seen that the p-side electrode **18** is in ohmic contact with the p-type contact layer **17B**. The contact resistivity continues to decrease with the processing time until 30 minutes has passed since the start of plasma processing. On and after the processing time exceeds 30 minutes, the contact resistivity is substantially constant at 3.0×10^{-4} Ωcm^2, which is about one-third as low as that of the conventional semiconductor device.

Also, as shown in FIG. **5**, the resistivity of the semiconductor laser device continues to decrease with the processing time until 30 minutes has passed since the start of plasma processing. On and after the processing time exceeds 30 minutes, the resistivity is substantially constant at 0.4 Ωcm, which is also about one-third as low as that of the conventional semiconductor device.

These results are obtained because the acceptor is activated according to this embodiment without conducting any heat treatment. That is to say, Mg can be activated uniformly within the entire crystal-growing planes of the p-type cladding and contact layers **16B** and **17B** without damaging the crystallinity thereof, thus increasing the mobility of holes. According to the results of experiments carried out by the present inventors, the mobility of holes when annealing was conducted to activate the acceptor at 600° C. or higher was about 10 $cm^2/Vsec$, while the mobility of holes was about 22 $cm^2/Vsec$ according to this embodiment.

If the plasma processing according to this embodiment is performed along with annealing, then the annealing temperature should be 500° C. or lower to prevent nitrogen atoms from detaching themselves from the crystals of respective nitrogen-containing semiconductor layers, specifically, the active layer **15**, p-type cladding layer **16B** and p-type contact layer **17B**, in particular.

Next, it will be described based on the results of several types of experiments how the acceptor can be activated in the p-type nitride semiconductor layers according to the method of this embodiment.

FIG. **6** illustrates respective photoluminescence intensities of the second Mg-doped layer **17A** that has not been processed with plasma yet and the p-type contact layer **17B** that has already been processed with plasma. In FIG. **6**, the curves **A1** and **B1** represent the photoluminescence intensities before and after the plasma processing, respectively. In this example, He—Cd laser light is used as exciting radiation to measure the photoluminescence intensity. As shown in FIG. **6**, a peak of emission resulting from Mg—H bonding appears on the curve **A1** at a wavelength of about 680 nm. On the other hand, a peak of emission resulting from the activation of the acceptor Mg due to the dissociation of H appears on the curve **B1** at a wavelength of about 470 nm. Thus, it can be seen that Mg, or the p-type dopant, can be activated as an acceptor by performing the plasma processing.

FIG. **7** illustrates respective dependence of a carrier (hole) density on an annealing temperature for the p-type contact layer **17B** processed with plasma by the method of the first embodiment and a p-type contact layer annealed by a conventional method. In FIG. **7**, the curves **B2** and **A2** represent a carrier density resulting from the inventive plasma processing for 40 minutes and a carrier density resulting the conventional annealing process at 600° C., respectively. These carrier densities were measured by a Hall method. As shown in FIG. **7**, when the substrate was annealed at about 600° C. according to the conventional method, the carrier density was about 2.2×10^{17} cm^{-3} as represented by the broken curve **A2**. In contrast, according to the method of the present invention, the carrier density increased to about 2.7×10^{17} cm^{-3} as represented by the solid curve **B2**. As can be seen, the carrier density can be increased according to this embodiment compared to the conventional method.

The second Mg-doped layer **17A** that had not been processed with plasma yet and the p-type contact layer **17B** that had been processed with plasma for 40 minutes were also analyzed in comparison by secondary ion mass spectroscopy (SIMS) although not shown. As a result, the present inventors confirmed that the concentration of hydrogen in the p-type contact layer **17B** that had already been processed with plasma decreased compared to the second Mg-doped layer **17A** that had not been exposed to plasma yet. Specifically, the concentration of hydrogen in the second Mg-doped layer **17A** was about 1.8×10^{19} cm^{-3}, while the concentration of hydrogen in the p-type contact layer **17B** was about 1.0×10^{19} cm^{-3}. In addition, no diffusion of Mg into the active layer **15** was observed, either.

Furthermore, when we analyzed the semiconductor laser device according to this embodiment using an electron microscope, almost no defects or cracking due to thermal hysteresis were observed unlike a conventional semiconductor device.

As can be seen, the results of various experiments and analyses prove that the inventive method for fabricating a semiconductor device, more specifically, the method for forming a p-type nitride semiconductor, is much superior to the conventional method.

The properties of the p-type semiconductor layer formed by the method of the present invention are superior to those obtained by the conventional method because of the following reasons:

(1) The surface of the second Mg-doped layer **17A** is exposed to the plasma, and no oxide film is formed thereon;

(2) The contaminants attached to the surface of the second Mg-doped layer **17A** can be removed by exposing the layer to the plasma, and the resulting p-type contact layer **17B** can have a cleaner surface; and

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List of the Patents in the Name of MEC

No.	Application No.	Filing Date	Patent No.	Date of Grant	Title
1	09/147462	12/30/1998	6,118,688	09/12/2000	FERROELECTRIC MEMORY DEVICE AND METHOD OF DRIVING THE SAME
2	09/147598	01/29/1999	6,157,563	12/05/2000	FERROELECTRIC MEMORY SYSTEM AND METHOD OF DRIVING THE SAME ** U.S. NATIONAL PHASE OF PCT/JP98/02883 FILED 06/26/98 **
3	09/285647	04/05/1999	6,099,390	08/08/2000	POLISHING PAD FOR SEMICONDUCTOR WAFER AND METHOD FOR POLISHING SEMICONDUCTOR WAFER
4	09/361219	07/27/1999	6,180,472	01/30/2001	METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
5	09/389024	09/02/1999	6,117,700	09/12/2000	METHOD FOR FABRICATING SEMICONDUCTOR DEVICE HAVING GROUP III NITRIDE

TOEITT 26538660

List of the Applications in the Name of MEC

No.	Application No.	Filing Date	Title
1	09/155420	09/29/1998	SEMICONDUCTOR LIGHT-EMITTING DEVICE, AND MANUFACTURING METHODS THEREFOR
2	09/557573	04/21/2000	LIGHT-EMITTING ELEMENT, SEMICONDUCTOR LIGHT-EMITTING DEVICE, AND MANUFACTURING METHODS THEREFOR
3	09/341918	07/21/1999	RESIN-MOLDED SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME ** U.S. NATIONAL PHASE OF PCT/JP98/00476 FILED 02/04/98 **
4	09/381381	09/20/1999	SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME
5	09/166904	10/06/1998	METHOD FOR CONTROLLING PRODUCTION LINE
6	09/477669	01/05/2000	NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR FABRICATING THE SAME
7	09/159594	09/24/1998	METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
8	09/160329	09/25/1998	PATTERN FORMATION METHOD
9	09/162232	09/29/1998	ELECTRONIC DEVICE AND METHOD FOR FABRICATING THE SAME
10	09/239949	01/29/1999	SEMICONDUCTOR DEVICE AND METHOD FOR DRIVING THE SAME
11	09/212411	12/16/1998	APPARATUS AND METHOD FOR PLASMA PROCESSING
12	09/243797	02/03/1999	METHOD FOR INTRODUCING IMPURITY INTO A SEMICONDUCTOR SUBSTRATE WITHOUT NEGATIVE CHARGE BUILDUP PHENOMENON
13	09/327468	06/08/1999	PATTERN FORMING METHOD
14	09/330018	06/11/1999	METHOD OF MANUFACTURING ELECTRONIC DEVICE
15	09/321713	05/28/1999	SEMICONDUCTOR DEVICE AND METHOD AND APPARATUS FOR FABRICATING THE SAME WHILE MINIMIZING OPERATING FAILURES AND OPTIMIZING YIELD
16	09/238584	01/28/1999	METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
17	09/289975	04/13/1999	AMPLIFYING SOLID-STATE IMAGING DEVICE, METHOD FOR DRIVING THE SAME, AND PHYSICAL QUANTITY DISTRIBUTION SENSING SEMICONDUCTOR DEVICE
18	09/321709	05/28/1999	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

List of the Applications in the Name of MEC

No.	Application No.	Filing Date	Title
19	09/249844	02/16/1999	METHOD OF FABRICATING INTERCONNECTS UTILIZING FLUORINE DOPED INSULATORS AND BARRIER LAYERS
20	09/289960	04/13/1999	METHOD FOR GROWING NITRIDE COMPOUND SEMICONDUCTOR
21	09/333050	06/15/1999	METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
22	09/321581	05/28/1999	SOLID STATE IMAGE DEVICE AND METHOD DRIVING THE SAME
23	09/317613	05/25/1999	CAPACITOR AND METHOD FOR FABRICATING THE SAME
24	09/317604	05/25/1999	METHOD FOR GROWING NITRIDE SEMICONDUCTOR CRYSTALS, NITRIDE SEMICONDUCTOR DEVICE, AND METHOD FOR FABRICATING THE SAME
25	09/366734	08/04/1999	CHARGED PARTICLE LITHOGRAPHY METHOD AND SYSTEM
26	09/292013	04/15/1999	SEMICONDUCTOR LASER DEVICE
27	09/417096	10/13/1999	PRODUCTION CONTROL SYSTEM AND METHOD
28	09/333048	06/15/1999	CMOS INVERTER AND STANDARD CELL USING THE SAME
29	09/338542	06/23/1999	SEMICONDUCTOR MEMORY
30	09/383418	08/26/1999	METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
31	09/345495	07/01/1999	SEMICONDUCTOR DEVICE AND METHOD FOR PROVIDING A CONTACT HOLE FORMED IN AN INSULATING FILM
32	09/327467	06/08/1999	METHOD FOR EXAMINING SEMICONDUCTOR SUBSTRATE, AND METHOD FOR CONTROLLING FABRICATION PROCESS OF SEMICONDUCTOR DEVICES
33	09/333049	06/15/1999	FERROELECTRIC MEMORY DEVICE
34	09/448438	11/24/1999	SEMICONDUCTOR STORAGE DEVICE AND METHOD OF MANUFACTURING THE SAME
35	09/383417	08/26/1999	APPARATUS AND METHOD FOR PLASMA ETCHING
36	09/419879	10/15/1999	TERMINAL LAND FRAME AND METHOD FOR MANUFACTURING THE SAME

No.	Application No.	Filing Date	Title
37	09/432125	11/02/1999	AMPLIFYING SOLID-STATE IMAGING DEVICE, AND METHOD FOR DRIVING THE SAME
38	09/432216	11/03/1999	LEADFRAME FOR USE IN MANUFACTURING A RESIN-MOLDED SEMICONDUCTOR DEVICE
39	09/420455	10/18/1999	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
40	09/417097	10/13/1999	AMPLIFYING SOLID-STATE IMAGING DEVICE, AND METHOD FOR DRIVING THE SAME
41	09/392584	09/09/1999	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
42	09/438584	11/12/1999	AMPLIFYING SOLID-STATE IMAGING DEVICE, AND METHOD FOR DRIVING THE SAME
43	09/447573	11/23/1999	APPARATUS AND METHOD FOR FEEDING SLURRY
44	09/731011	12/07/2000	APPARATUS AND METHOD FOR FEEDING SLURRY
45	09/479847	01/10/2000	COMPOSITE LIGHT-EMITTING DEVICE, SEMICONDUCTOR LIGHT-EMITTING UNIT AND METHOD FOR FABRICATING THE UNIT
46	09/480942	01/11/2000	BIPOLAR TRANSISTOR AND METHOD OF FABRICATING THE SAME
47	09/450512	11/30/1999	METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
48	09/570545	05/12/2000	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
49	09/456381	12/08/1999	METHOD OF MEASURING TEMPERATURE, METHOD OF TAKING SAMPLES FOR TEMPERATURE MEASUREMENT AND METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
50	09/551880	04/18/2000	LITHOGRAPHY PATTERN DATA GENERATION METHOD, LITHOGRAPHY PATTERN FABRICATION METHOD AND CHARGED PARTICLE LITHOGRAPHY SYSTEM
51	09/560299	04/27/2000	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME
52	09/515673	02/29/2000	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
53	09/511371	02/23/2000	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME
54	09/576971	05/24/2000	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

No.	Application No.	Filing Date	Title
55	09/592266	06/13/2000	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME
56	09/639157	08/16/2000	METHOD OF MAKING FERROELECTRIC THIN FILM, FERROELECTRIC CAPICITOR, FERROELECTRIC MEMORY AND METHOD FOR FABRICATING FERROELECTRIC MEMORY
57	09/613631	07/11/2000	ECC CIRCUIT-CONTAINING SEMICONDUCTOR MEMORY DEVICE AND METHOD OF TESTING THE SAME
58	09/552622	04/19/2000	METHOD AND APPARATUS FOR REJUVENATING POLISHING SLURRY
59	09/526174	03/15/2000	METHOD OF CLEANING ELECTRONIC DEVICE AND METHOD OF FABRICATING THE SAME
60	09/551541	04/18/2000	METHOD OF FABRICATING SEMICONDUCTOR DEVICE
61	09/551542	04/18/2000	METHOD OF FABRICATING SEMICONDUCTOR DEVICE
62	09/570391	05/12/2000	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME
63	09/679617	10/05/2000	METHOD OF FORMING ELECTRODE STRUCTURE AND METHOD OF FABRICATING SEMICONDUCTOR DEVICE
64	09/680053	10/05/2000	METHOD OF FORMING ELECTRODE STRUCTURE AND METHOD OF FABRICATING SEMICONDUCTOR DEVICE
65	09/633234	08/04/2000	SEMICONDUCTOR LIGHT-EMITTING UNIT, OPTICAL HEAD APPARATUS AND OPTICAL DISK SYSTEM
66	09/615744	07/13/2000	PHOTOMASK, RESIST PATTERN FORMATION METHOD, METHOD OF DETERMINING ALIGNMENT ACCURACY AND METHOD OF FABRICATING SEMICONDUCTOR DEVICE
67	09/680978	10/06/2000	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME
68	09/661369	09/13/2000	METHOD OF FABRICATING SEMICONDUCTOR DEVICE
69	09/654070	09/01/2000	LEADFRAME AND METHOD FOR MANUFACTURING RESIN-MOLDED SEMICONDUCTOR DEVICE
70	09/639160	08/16/2000	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
71	09/688197	10/16/2000	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME
72	09/664555	09/18/2000	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

No.	Application No.	Filing Date	Title
73	09/662359	09/15/2000	METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
74	09/662358	09/15/2000	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
75	09/649573	08/29/2000	METHOD FOR DETERMINING A PRECEDING WAFER, METHOD FOR DETERMINING A MEASURING WAFER, AND METHOD FOR ADJUSTING THE NUMBER OF WAFERS
76	09/640519	08/17/2000	METHOD OF FABRICATING SEMICONDUCTOR DEVICE
77	09/688196	10/16/2000	METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
78	09/630680	08/01/2000	PLASMA PROCESSING METHOD
79	09/666156	09/19/2000	HIGH-VOLTAGE MOS TRANSISTOR AND METHOD FOR FABRICATING THE SAME
80	09/729202	12/05/2000	METHOD FOR FABRICATING AN ELECTRONIC DEVICE
81	09/672860	09/29/2000	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
82	09/726654	12/01/2000	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
83	09/662004	09/14/2000	METHOD OF FORMING INSULATING FILM AND METHOD OF FABRICATING SEMICONDUCTOR DEVICE
84	09/680054	10/05/2000	SEMICONDUCTOR DEVICE, SEMICONDUCTOR SUBSTRATE, AND MANUFACTURE METHOD
85	09/661370	09/13/2000	FERROELECTRIC MEMORY DEVICE
86	09/695381	10/25/2000	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
87	09/707844	11/08/2000	SEMICONDUCTOR DEVICE
88	09/729424	12/05/2000	NITRIDE SEMICONDUCTOR DEVICE
89	09/708084	11/08/2000	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
90	09/708082	11/08/2000	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

TOSHIBA CORPORATION

List of the Applications in the Name of MEC

No.	Application No.	Filing Date	Title
91	09/708086	11/08/2000	METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
92	09/708085	11/08/2000	METHOD FOR FABRICATING SEMICONDUCTOR DEVICE
93	09/758287	01/12/2001	METHOD FOR GROWING NITRIDE SEMICONDUCTOR CRYSTALS, NITRIDE SEMICONDUCTOR DEVICE, AND METHOD FOR FAVRICATING THE SAME
94	09/714130	11/17/2000	METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE
95	09/735792	12/14/2000	PRINTED WIRING BOARD, IC CARD MODULE USING THE SAME, AND METHOD FOR PRODUCING IC CARD MODULE
96	09/734176	12/12/2000	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
97	09/745412	12/26/2000	SEMICONDUCTOR DEVICE AND METHOD FOR THE FABRICATION THEREOF
98	09/785503	02/20/2001	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATION THEREOF
99	09/735793	12/14/2000	SEMICONDUCTOR LIGHT EMITTER AND METHOD FOR FABRICATING THE SAME
100	09/783307	02/15/2001	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

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This will acknowledge receipt of the following:

1. Recordation Form Cover Sheet for Merger
2. English Translation of Japanese Certified Extract Copy of Register
3. Japanese Certified Extract Copy of Register
4. List of Application Numbers and Patents Numbers in the Name of MEC
5. Check No. 16803 in the amount of $4200.00 (merger recordation)

Merger of Matsushita Electronics Corporation
with Matsushita Electric Industrial Co., Ltd.

Docket: 740819-0
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